I2C Core APB User Guide

# Registers

## Addresses

|  |  |  |
| --- | --- | --- |
| PADDR | Register Name | Description |
| 0x00 | CTRL | Control Register, used to configure the I2C core |
| 0x01 | DATA | Data Register, I2C read/write data |
| 0x02 | CLK0 | Clock Divider bits [7 - 0] |
| 0x03 | CLK1 | Clock Divider bits [15 – 8] |
| 0x10 | AUTO CTRL | Auto Control Register, used to configure automated I2C sequence |
| 0x8X | AUTO DATA | Data bits of Auto Sequence Register [7 - 0] |
| 0xCX | AUTO OPcode | Opcode bits of Auto Sequence Register [9 - 8] |

## Control Register

|  |  |  |
| --- | --- | --- |
| Bit | R/W | Function |
| 7 | R | 0 : I2C bus is idle  1 : I2C bus is busy by either this core or some other I2C master |
| 6 - 5 | R | I2C Core Status  00 : Idle  01 : Busy doing action according to bits 4-2  10 : Interrupt active, waiting for next command, holding I2C bus  11 : Interrupt active with ACK failed, waiting for next command, holding I2C bus |
| 4 - 2 | W | 000 : NOP, No change to SDA or SCL but Interrupt will fire after 1 I2C clock  001 : Start, if I2C bus is idle, Start event will be sent.  010 : Stop, if status shows this I2C is in control, Stop signal will be sent.  011 : Repeated Start, if status shows this I2C is in control, RStart signal will be sent.  100 : Data will be written to the I2C bus, SDA Enable is enabled.  101 : Data will be read from the I2C bus, SDA Enable is disabled. |
| 1 | W | 0 : This I2C core is idle/listening  1 : Initiate I2C event with this I2C core, will be set to 0 upon completion |
| 0 | W | 0 : I2C core is disabled. Will neither transmit nor monitor I2C bus.  1 : I2C core is enabled.  \* Toggling this is like a soft reset. Probably. |

## Data Register

|  |  |  |
| --- | --- | --- |
| Bit | R/W | Function |
| 7 - 0 | R/W |  |

## Clock Divider

|  |  |  |
| --- | --- | --- |
| Bit | R/W | Function |
| 15 - 0 | R/W |  |

## Auto Control Register

|  |  |  |
| --- | --- | --- |
| Bit | R/W | Function |
| 7 - 2 | R | 000000 – 111111 : Sequence counter capable of indicating up to 64 registers. Sequences longer than this are able to be configured in which case this becomes inaccurate. |
| 1 | W | 0 : Automatic polling is idle.  1 : Initiate an Automatic Sequence. |
| 0 | W | 0 : Automatic polling is off.  1 : Automatic polling is enabled.  \* If set to 1, an interrupt signal may be used to trigger the automatic sequence |

## Auto Sequence Register

|  |  |  |
| --- | --- | --- |
| Bit | R/W | Function |
| 9 - 8 | W | 00 : No Operation, used to identify unused registers.  01 : bits 7-0 identify special conditions such as START, STOP, etc.  10 : data in bits 7-0 are to be written to the I2C bus  11 : data in bits 7-0 are to be read from the I2C bus |
| 7 - 0 | W | Bits to be read or written to the I2C bus where 7 is the MSB  If bit 9 = 1:  0b00000001 = START  0b00000010 = STOP  0b00000011 = REPEATED START |